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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,797	06/02/2006	Yang Yang	58086-231274	4944
26694	7590	09/08/2008	EXAMINER	
VENABLE LLP P.O. BOX 34385 WASHINGTON, DC 20043-9998				TRAN, LONG K
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/581,797	YANG ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	LONG K. TRAN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-22 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1-22 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date ____ .	6) <input type="checkbox"/> Other: ____ .

**DETAILED ACTION*****Response to Amendment***

1. This office action is in response to Amendment filed on 05/21/2008.
2. Independent claims **1, 5 and 12** have been amended.
3. Claims **17 – 22** have been added.
4. Claims **1 – 22** are presented for examination.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **1, 2, 4, 5, 6, 7, 8, 12, 13, 14 and 15** are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al. (US 6,600,473).

Regarding claims **1, 2, 5, 6 and 7**, Kobayashi, figures 1 – 26, discloses an electrical bistable device (*the photoconductive switching is connected electrically to and/or combined with a functional element such as a display element showing a memory characteristic, a bistable liquid crystal display element, emphasis added by examiner*) in a memory device and a method of making the device comprising:

An electrically conductive mixed layer (12) comprising a first side and a second side (not labeled), the mixed layer comprising a low conductivity material and a sufficient amount of a high conductivity material, formed of material

selected from a group consisting of metals, metal oxides, conducting polymers and organic conductors, wherein the mixed layer is electrically conductive (column 6, lines 40 - 67; column 8, lines 18 – 29);

A first and a second layer (10), (14) of low conductivity material, formed of material selected from a group consisting of organic semiconductor and organic insulators, on each side of the electrically conductive mixed ((12); column 7, lines 49 - 57), respectively;

A first and a second electrode 16, 18 (fig. 1) attached on first and second side of the low conductivity material 10 and 14, respectively;

A first interface (not labeled) located on the first side of the mixed layer where the first layer of low conductivity material and the mixed layer meet, the first interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage between the first electrode (16) and the mixed layer. It is to be noted that the bistable body of Kobayashi's device would including the first interface, the electrically conductive mixed layer, the second interface, emphasis added by examiner.

Regarding claims **12, 13 and 14**, Kobayashi, figures 1 – 26, discloses an electrical bistable device in a memory device and a method of making the device comprising:

An electrically conductive mixed layer (12) comprising a first side and a second side (not labeled), the mixed layer comprising a low conductivity material and a sufficient amount of a high conductivity material, formed of material selected from a group consisting of metals, metal oxides, conducting polymers

and organic conductors, wherein the mixed layer is electrically conductive (column 3, lines 24 – 31, column 6, lines 40 - 67; column 8, lines 18 – 29);

A first layer (10) of low conductivity material, formed of material selected from a group consisting of organic semiconductor and organic insulators, on the first side of the electrically conductive mixed ((12); column 7, lines 49 - 57), having a first electrode side;

A second layer (14) of low conductivity material, formed of material selected from a group consisting of organic semiconductor and organic insulators, on the first side of the electrically conductive mixed ((12); column 7, lines 49 - 57), having a second electrode side.

A first interface located on the first side of the mixed layer where the first layer of low conductivity material and the mixed layer meet, the first interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage to the first interface (column 8, lines 41+);

A second interface located on the second side of the mixed layer where the second layer of low conductivity material and the mixed layer meet, the second interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage to the second interface (column 8, lines 41+);

A first and a second electrode 16, 18 (fig. 1) attached on first and second side of the low conductivity material 10 and 14, respectively;

A memory input element (column 3, lines 32 – 59) for applying a voltage to

said first electrode, said second electrode and/or said electrically conductive mixed layer to convert said first interface and/or said second interfaces between said low electrical resistance state and said high electrical resistance state; and

a memory readout element which provides and indication of whether said first interface and/or said second interface is in said low electrical resistance state or said high electrical resistance state (column 4, lines 3 +).

Regarding claims **4, 8 and 15**, Kobayashi discloses the electrically conductive mixed layer is formed by vacuum deposition or sputtering or a spin coating process or dipping process (column 8, lines 30 – 33).

7. Claims **1 – 22** are rejected under 35 U.S.C. 102(b) as being anticipated by Yang et al. (WO 02/37500)

Regarding claims **1 and 5 – 11**, Yang, figures 1 – 17, discloses: an electrical bistable device in a memory device and a method of making the device ([0030]) comprising:

An electrically conductive mixed layer (30) comprising a first side and a second side , the mixed layer comprising a low conductivity material and a high conductivity material wherein the mixed layer is electrically conductive ([0034]); “It is also contemplated within the present invention that the bistable body may include multiple layers of high conductivity material located between alternating layers of low conductivity material”;

A first and a second layer (32), (34) of low conductivity material on each side of the electrically conductive mixed ((30), [0034]), respectively;

A first and a second electrode (36), (42) attached on first and second side of the low conductivity material, respectively;

A first interface (not labeled) located on the first side of the mixed layer where the first layer of low conductivity material and the mixed layer meet, the first interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage between the first electrode and the mixed layer (claim 1).

A second interface (not label) located on the second side of the mixed layer where the first layer of low conductivity material and the mixed layer meet, the second interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage between the first electrode and the mixed layer (claim 1).

It is to be noted that the bistable body of Yang's device would including the first interface, the electrically conductive mixed layer, the second interface, emphasis added by examiner.

Regarding claim 2, Yang discloses the low conductivity material is selected from the group cosisting of organic semiconductor and organic insulators (claim 4).

Regarding claim 3, Yang discloses the high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors (claim 5).

Regarding claim 4, Yang discloses the electrically conductive mixed layer (bistable body) is formed by condensing vapors of the high conductivity and low

conductivity materials together to form the electrically conductive mixed layer (bistable body).

Regarding claims **12 – 16**, Yang, figures 1 – 17, discloses a memory device comprising:

An electrically conductive mixed layer (30) comprising a first side and a second side, the mixed layer comprising a low conductivity material and a high conductivity material wherein the mixed layer is electrically conductive ([0034]); “It is also contemplated within the present invention that the bistable body may include multiple layers of high conductivity material located between alternating layers of low conductivity material”);

A first and a second layer (32), (34) of low conductivity material on each side of the electrically conductive mixed (30), [0034]), respectively;

A first and a second electrode (36), (42) attached on first and second side of the low conductivity material, respectively;

A first interface (not labeled) located on the first side of the mixed layer where the first layer of low conductivity material and the mixed layer meet, the first interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage between the first electrode and the mixed layer (claim 15).

A second interface located (not label)on the second side of the mixed layer where the first layer of low conductivity material and the mixed layer meet, the second interface being electrically convertible between a low resistance state and a high resistance state by application of an electrical voltage between the

first electrode and the mixed layer (claim 15).

A memory readout element which provides an indication of whether the first interface and/or the second interface (body of the bistable including the first interface, the electrically mixed layer, and the second interface, emphasis added by the examiner) is in the low electrical resistance state or the high electrical resistance (claim 15)

Regarding claim 13, Yang discloses the low conductivity material is selected from the group consisting of organic semiconductor and organic insulators (claim 4).

Regarding claim 14, Yang discloses the high conductivity material is selected from the group consisting of metals, metal oxides, conducting polymers and organic conductors (claim 5).

Regarding claim 15, Yang discloses the electrically conductive mixed layer (bistable body) is formed by condensing vapors of the high conductivity and low conductivity materials together to form the electrically conductive mixed layer (bistable body).

Regarding claim 16, Yang discloses the step of applying a sufficient electrical voltage across said first and second electrodes of said memory device to convert said bistable body between said high resistance state and said low resistance state (claim 27). It is to be noted that limitations “method of operating a memory device...” are ***functional and/or operating languages*** and the claimed invention is an apparatus (device) and making an apparatus (device). The apparatus and method of

making must be distinguished from the prior art in term of structure and making rather than function. See part of MPEP § 2114 [R-1] that states: *While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). “[A]pparatus claims cover what a device is, not what a device does.” Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).*

Regarding claims **17, 19, 20** and **21**, Yang discloses the electrically conductive mixed layer is a two-phase system consisting essentially of electrically conductive nanoparticles dispersed in said low conductivity material ([009], [0033])).

Regarding claims **18** and **22**, Yang discloses electrically conductive nanoparticles have an average particle size of at least 1 nm and less than 50 nm ([0041]).

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims **9 – 11** and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (US 6,600,473) in view of remarks.

Regarding claims **9 – 11** and **16**, Kobayashi discloses the claimed inventions of claim 1 or claim 12, respectively, and a pulse unit for applying a negative pulse and positive pulse to provide voltage of the electrode on the display element side being higher than that of the electrode of the photoconductive switching element side of the device (column 4, lines 33+), but does not explicitly teach applying a sufficient voltage between the first and second electrodes to convert both first interface and second interface between a high resistance state and low resistance state. However, the limitation “applying a sufficient electrical voltage” is ***functional languages*** and the claimed invention is an apparatus (device) and making an apparatus (device). The apparatus and method of making must be distinguished from the prior art in term of structure and making rather than function. See part of MPEP § 2114 [R-1] that states:

*While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board’s finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent*

*in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). “[A]pparatus claims cover what a device is, not what a device does.” Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).*

### ***Response to Arguments***

9. Applicant's arguments with respect to claims 1 – 16 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

10. Applicant's amendment (and with new claims) necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LONG K. TRAN whose telephone number is (571)272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Long K. Tran/  
Primary Examiner, A.U. 2818

August 21, 2008